IN THE CLAIMS:

All of the pending claims 1 through 72 are presented below. New claims 49 through 72 have been added. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Original) A method for forming a conductive via in a semiconductor component, comprising:

providing a substrate having a first surface and an opposing, second surface;

forming at least one hole through the substrate defined by a sidewall and extending from the first surface of the substrate to the opposing, second surface of the substrate;

applying a seed layer to the first surface of the substrate, the opposing, second surface of the substrate and the sidewall of the at least one hole;

removing the seed layer overlying the first surface and the opposing, second surface of the substrate;

coating the seed layer on the sidewall of the at least one hole with a conductive layer; and

introducing a filler material into a remaining space within the at least one hole.

2. (Original) The method of claim 1, wherein forming the at least one hole through the substrate is effected by at least one of laser ablation, dry etching and wet etching.

3. (Original) The method of claim 1, further comprising cleaning the sidewall defining the at least one hole prior to applying the seed layer.

4. (Previously Presented) The method of claim 1, further comprising forming an insulative layer on the first surface, the opposing, second surface and the sidewall defining the at least one hole prior to applying the seed layer.

5. (Original) The method of claim 1, further comprising forming at least one bond pad overlying at least a portion of the conductive via on at least one of the first surface and the opposing, second surface after introducing the filler material.

6. (Original) The method of claim 1, wherein applying the seed layer comprises depositing conductive material using a chemical vapor deposition process, a physical vapor deposition process, an atomic layer deposition process, a plasma enhanced chemical vapor deposition process, vacuum evaporation or sputtering.

7. (Original) The method of claim 1, wherein removing the seed layer overlying the first surface and the opposing, second surface of the substrate is effected by abrasive planarization.

8. (Original) The method of claim 1, wherein coating the seed layer with the conductive layer comprises electrolessly plating the seed layer with a metal material.

9. (Original) The method of claim 1, wherein introducing the filler material into the remaining space of the at least one hole comprises one of spin coating spin-on-glass into the remaining space, depositing polysilicon into the remaining space using a diffusion process or depositing solder paste or a solder alloy into the remaining space.

10. (Original) The method of claim 1, wherein introducing the filler material comprises introducing either a conductive or a nonconductive filler material.

11. (Previously Presented) The method of claim 1, further comprising:
applying a layer of resist overlying the seed layer; and
after removal of the seed layer, removing the layer of resist.

12. (Original) A method for forming a conductive via in a substrate comprising:
providing a substrate having a first surface and an opposing, second surface;
forming at least one cavity in the first surface of the substrate;
applying a conductive layer to an exposed area of the substrate defining the at least one cavity;
introducing a filler material into a remaining space of the at least one cavity; and
removing material of the substrate from the opposing, second surface of the substrate to a depth sufficient to expose the conductive layer and the filler material introduced into the at least one cavity.

13. (Original) The method of claim 12, wherein forming the at least one cavity in the first surface is effected by at least one of laser ablation, dry etching and wet etching.

14. (Original) The method of claim 12, further comprising cleaning the exposed area of the substrate defining the at least one cavity prior to applying the conductive layer.

15. (Original) The method of claim 12, further comprising forming an insulative layer on the first surface and the exposed area defining the at least one cavity prior to applying the conductive layer.

16. (Previously Presented) The method of claim 12, further comprising forming at least one bond pad overlying at least a portion of the conductive via on at least one of the first surface and the opposing, second surface of the substrate.

17. (Previously Presented) The method of claim 12, wherein applying the conductive layer comprises:
depositing a seed layer on the first surface of the substrate and the exposed area of the substrate defining the at least one cavity;
removing the seed layer overlying the first surface of the substrate; and

coating the seed layer on the exposed area defining the at least one cavity with the conductive layer.

18. (Previously Presented) The method of claim 17, wherein depositing the seed layer comprises depositing a conductive material using a chemical vapor deposition process, a physical vapor deposition process, an atomic layer deposition process, a plasma enhanced chemical vapor deposition process, vacuum evaporation or sputtering.

19. (Original) The method of claim 17, wherein removing the seed layer overlying the first surface of the substrate is effected by abrasive planarization.

20. (Original) The method of claim 17, wherein coating the seed layer with the conductive layer comprises electrolessly plating the seed layer with a metal material.

21. (Original) The method of claim 12, wherein introducing the filler material comprises spin coating spin-on-glass into the remaining space, depositing polysilicon into the remaining space using a diffusion process or depositing solder paste or a solder alloy into the remaining space.

22. (Original) The method of claim 12, wherein removing the material of the substrate from the opposing, second surface is effected by abrasive planarization.

23. (Original) The method of claim 12, wherein introducing the filler material comprises introducing either a conductive or a nonconductive filler material.

24. (Previously Presented) The method of claim 12, further comprising:

covering the first surface of the substrate with a barrier layer prior to forming the at least one cavity; and

wherein applying the conductive layer comprises:

depositing a seed layer only on the exposed area of the substrate defining the at least one cavity; and

coating the seed layer on the exposed area defining the at least one cavity with the conductive layer.

25. (Previously Presented) An intermediate semiconductor component, comprising:

a substrate having a first surface and an opposing, second surface; and

at least one via extending into the first surface of the substrate and terminating short of the opposing, second surface;

wherein the at least one via comprises an annular conductive layer that extends from the first surface and circumscribes a filler material.

26. (Original) The intermediate semiconductor component of claim 25, wherein the annular conductive layer comprises a metal layer formed on a seed layer, wherein the seed layer is located between the metal layer and the substrate.

27. (Original) The intermediate semiconductor component of claim 25, wherein the filler material is selected from the group consisting of spin-on-glass, polysilicon, solder paste and a solder alloy.

28. (Original) The intermediate semiconductor component of claim 25, wherein the filler material is either a conductive or a nonconductive filler material.

29. (Previously Presented) The intermediate semiconductor component of claim 26, wherein the seed layer is selected from the group consisting of titanium nitride, titanium, tantalum nitride, copper, silicon nitride, and a polysilicon.

30. (Original) The intermediate semiconductor component of claim 26, wherein the metal layer is selected from the group of metals consisting of nickel, cobalt, copper, silver, titanium, iridium, gold, tungsten, tantalum, molybdenum, platinum, palladium, nickel-phosphorus, palladium-phosphorus, cobalt-phosphorus, a Co-W-P alloy, alloys of the foregoing metals and mixtures of any of the foregoing.

31. (Original) The intermediate semiconductor component of claim 25, further comprising an insulative layer located between the annular conductive layer and the substrate.

32. (Original) The intermediate semiconductor component of claim 25, further comprising a barrier layer on the first surface.

33. (Original) A semiconductor component, comprising:
a substrate having a first surface and an opposing, second surface; and
at least one via, comprising:
an annular conductive layer extending from the first surface of the substrate to the opposing, second surface of the substrate; and
a silicon-containing filler material circumscribed by the annular conductive layer.

34. (Previously Presented) The semiconductor component of claim 33, further comprising at least one bond pad overlying at least a portion of the at least one via on at least one of the first surface and the opposing, second surface of the substrate.

35. (Original) The semiconductor device of claim 33, wherein the annular conductive layer is metal.

36. (Original) The semiconductor device of claim 33, wherein the silicon-containing filler material is spin-on-glass or polysilicon.

37. (Original) The semiconductor component of claim 33, wherein the annular conductive layer comprises an electroless plated metal layer and a seed layer, wherein the seed layer is located between the electroless plated metal layer and the substrate.

38. (Original) The semiconductor component of claim 37, wherein the seed layer comprises a conductive material selected from the group of conductive materials consisting of titanium nitride, titanium, tantalum nitride, copper, and silicon nitride.

39. (Original) The semiconductor device of claim 37, wherein the electroless plated metal layer is selected from the group of metals consisting of nickel, cobalt, copper, silver, titanium, iridium, gold, tungsten, tantalum, platinum, palladium, molybdenum, nickel-phosphorus, palladium-phosphorus, cobalt-phosphorus, a Co-W-P alloy, alloys of the foregoing metals and mixtures of any of the foregoing.

40. (Original) The semiconductor component of claim 33, further comprising an insulative layer located between the annular conductive layer and the substrate.

41. (Original) A system comprising:

a microprocessor; and

at least one memory device in communication with the microprocessor comprising:

a substrate having a first surface and an opposing, second surface; and

at least one via, comprising:

an annular layer of a conductive material extending from the first surface of the substrate to the opposing, second surface of the substrate; and

a silicon-containing filler material circumscribed by the annular layer of the conductive material, the filler material extending from the first surface of the substrate to the opposing, second surface of the substrate.

42. (Previously Presented) The system of claim 41, wherein the at least one memory device further comprises at least one bond pad overlying at least a portion of the at least one via on at least one of the first surface and the opposing, second surface of the substrate.

43. (Original) The system of claim 41, wherein the annular layer of the conductive material is metal.

44. (Original) The system of claim 41, wherein the silicon-containing filler material is spin-on-glass or polysilicon.

45. (Original) The system of claim 41, wherein the annular layer of the conductive material comprises an electroless plated metal layer and a seed layer.

46. (Original) The system of claim 45, wherein the seed layer comprises a conductive material selected from the group of conductive materials consisting of titanium nitride, titanium, tantalumn nitride, copper, and silicon nitride.

47. (Original) The system of claim 45, wherein the electroless plated metal layer is selected from the group of metals consisting of nickel, cobalt, copper, silver, titanium, iridium, gold, tungsten, tantalum, molybdenum, platinum, palladium, nickel-phosphorus, palladium-phosphorus, cobalt-phosphorus, a Co-W-P alloy, alloys of the foregoing metals and mixtures of any of the foregoing.

48. (Original) The system of claim 41, further comprising a passivation layer located between the annular layer and the substrate.

49. (New) A method for forming a conductive via in a semiconductor component, comprising:

providing a substrate having a first surface and an opposing, second surface;

forming at least one hole through the substrate defined by a sidewall and extending from the first surface of the substrate to the opposing, second surface of the substrate; and

introducing a conductive filler material comprising a solder alloy into the at least one hole.

50. (New) The method of claim 49, wherein the solder alloy is introduced into the at least one via by flowing in a molten state.

51. (New) The method of claim 49, wherein the solder alloy is introduced into the at least one via by screen printing.

52. (New) The method of claim 49, wherein forming the at least one hole through the substrate is effected by at least one of laser ablation, dry etching and wet etching.

53. (New) The method of claim 49, further comprising cleaning the sidewall defining the at least one hole prior to introducing the conductive filler material.

54. (New) The method of claim 49, further comprising forming an insulative layer on the first surface, the opposing, second surface and the sidewall defining the at least one hole prior to introducing the conductive filler material.

55. (New) The method of claim 49, further comprising forming at least one bond pad overlying at least a portion of the conductive via on at least one of the first surface and the opposing, second surface after introducing the conductive filler material.

56. (New) A method for forming a conductive via in a substrate comprising:

providing a substrate having a first surface and an opposing, second surface;

forming at least one cavity in the first surface of the substrate;

introducing a conductive filler material comprising a solder alloy into a remaining space of the at least one cavity; and

removing material of the substrate from the opposing, second surface of the substrate to a depth sufficient to expose the conductive filler material introduced into the at least one cavity.

57. (New) The method of claim 56, wherein the solder alloy is introduced into the at least one via by flowing in a molten state.

58. (New) The method of claim 56, wherein the solder alloy is introduced into the at least one via by screen printing.

59. (New) The method of claim 56, wherein forming the at least one cavity in the first surface is effected by at least one of laser ablation, dry etching and wet etching.

60. (New) The method of claim 56, further comprising cleaning the exposed area of the substrate defining the at least one cavity prior to introducing the conductive filler material.

61. (New) The method of claim 56, further comprising forming an insulative layer on the first surface and the exposed area defining the at least one cavity prior to introducing the conductive filler material.

62. (New) The method of claim 56, further comprising forming at least one bond pad overlying at least a portion of the conductive via on at least one of the first surface and the opposing, second surface of the substrate.

63. (New) The method of claim 56, wherein removing the material of the substrate from the opposing, second surface is effected by abrasive planarization.

64. (New) An intermediate semiconductor component, comprising:
a substrate having a first surface and an opposing, second surface; and
at least one via extending into the first surface of the substrate and terminating short of the

opposing, second surface;

wherein the at least one via includes conductive filler material comprising a solder alloy that extends from the first surface.

65. (New) The intermediate semiconductor component of claim 64, further comprising an insulative layer located between the conductive filler material and the substrate.

66. (New) The intermediate semiconductor component of claim 64, further comprising a barrier layer on the first surface.

67. (New) A semiconductor component, comprising:

a substrate having a first surface and an opposing, second surface; and

at least one via, comprising:

a conductive filler material comprising a solder alloy extending from the first surface of the substrate to the opposing, second surface of the substrate.

68. (New) The semiconductor component of claim 67, further comprising at least one bond pad overlying at least a portion of the at least one via on at least one of the first surface and the opposing, second surface of the substrate.

69. (New) The semiconductor component of claim 67, further comprising an insulative layer located between the conductive filler material and the substrate.

70. (New) A system comprising:

a microprocessor; and

at least one memory device in communication with the microprocessor comprising:

a substrate having a first surface and an opposing, second surface; and

at least one via, comprising:

a conductive filler material comprising a solder alloy extending from the first surface of the substrate to the opposing, second surface of the substrate.

71. (New) The system of claim 70, wherein the at least one memory device further comprises at least one bond pad overlying at least a portion of the at least one via on at least one of the first surface and the opposing, second surface of the substrate.

72. (New) The system of claim 70, further comprising a passivation layer located between the conductive filler material and the substrate.